

Exhibit F

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Paper 8
Entered: June 7, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR
PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00203
Patent 7,619,912 B2

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

JURGOVAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314
Granting Motion for Joinder
35 U.S.C. § 315(c); 37 C.F.R. § 42.122

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I. INTRODUCTION

A. *Background*

Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively, “Petitioner”) filed a Petition (Paper 3, “Pet.”) requesting *inter partes* review of claim 16 of U.S. Patent No. 7,619,912 B2 (Ex. 1001, “’912 patent”). Netlist, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). In IPR2022-00615 (“615 IPR”), we instituted *inter partes* review of claim 16 of the ’912 patent based on a petition filed by Samsung Electronics Co., Ltd. (“Samsung”). 615 IPR, Papers 1, 20. In this proceeding, Petitioner concurrently filed the Petition and a Motion for Joinder (Paper 1, “Motion”) seeking to be joined as a petitioner in the 615 IPR. Petitioner represents that Samsung, the petitioner in the 615 IPR, does not oppose joinder. Motion 2. Patent Owner did not file an opposition to the Motion.

In its Preliminary Response, Patent Owner presents arguments or evidence that were not made in the 615 IPR, which we address below.

B. *Related Matters*

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters, including the 615 IPR, which Petitioner seeks to join. Pet. 1–2; Paper 5 at 1–2.

C. *Real Parties in Interest*

The Petitioner entities name themselves as real parties-in-interest in this case. Pet. 1. Patent Owner names itself as the real party-in-interest. Paper 5, 1.

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D. Challenged Claim

Independent claim 16, which is the only claim that is challenged in this proceeding, is reproduced below with Petitioner's limitation identifiers in brackets. *See* Pet. ix–x.

[16.pre] A memory module connectable to a computer system, the memory module comprising:

[16.a] a printed circuit board;

[16.b] a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, [16.b.i] the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

[16.c] a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, [16.c.i] the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, [16.c.ii] the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, [16.c.iii] the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, [16.c.iv] wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

[16.d] a phase-lock loop device coupled to the printed circuit board, [16.d.i] the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

[16.e] wherein the command signal is transmitted to only

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one DDR memory device at a time.

Ex. 1001, *Inter Partes* Reexamination Certificate, 3:9–43.

E. Asserted Grounds of Unpatentability

Petitioner presents the following grounds, which are identical to the instituted grounds in the 615 IPR:

| Claim(s) Challenged | 35 U.S.C. § | Reference(s)/Basis |
|------------------------|---------------------|--------------------------------|
| 16 | 103(a) ¹ | Perego-422, ² |
| 16 | 103(a) | Perego-422, Amidi ³ |
| 16 | 103(a) | Ellsberry ⁴ |

Pet. 3; *see* 615 IPR, Paper 20 at 7, 59 (identifying same grounds and instituting *inter partes* review).

II. ANALYSIS

A. Claim Construction

Patent Owner argues that the '912 patent consistently uses the term “rank” to include multiple memory devices, not just one memory device. Prelim. Resp. 5–11. Patent Owner contends that claim 16 of the '912 patent is directed to a DDR memory module which requires multiple devices per rank. *Id.* at 5–6. Patent Owner contends that Petitioner’s argument that a

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. For this proceeding, Petitioner assumes that the '912 patent has an effective priority date before this date (Pet. 2) and applies the pre-AIA version of § 103.

² US 7,363,422 B2, issued April 22, 2008 (Ex. 1035).

³ US 2006/0117152 A1, published June 1, 2006 (Ex. 1036).

⁴ US 2006/0277355 A1, published December 7, 2006 (Ex. 1037).

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rank can include only one memory device derives from its argument against Patent Owner's US 9,858,215 B1 (Ex. 2109, "the '215 patent") which uses the term "memory integrated circuits" and not "ranks." Prelim. Resp. 8–11. Patent Owner further relies on Petitioner's declarant, Dr. Wolfe, from the 615 IPR, who testified that in forty years he had never heard of a memory module with DDR or new generations of DRAMs having a width less than 16 bits, implying that they would include multiple memory devices per rank. *Id.* at 10. Patent Owner also argues that the extrinsic evidence supports its interpretation of "rank" because Petitioner's website refers to ranks as including multiple DRAM components, Petitioner's employee in the 615 IPR presented a JEDEC proposal and vehemently disagreed that a rank of memory could be a single DRAM, and the Jacob textbook allegedly defines "rank" to require multiple devices because it describes them as operating in lockstep in response to a command. *Id.* at 11–14.

Petitioner contends that the '912 patent discloses a single-device "rank" embodiment. Pet. 7. Specifically, the '912 patent states the following:

In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices.

Ex. 1001, 8:48–57. Petitioner contends that this excerpt from the '912 patent supports that a rank can be composed of only one memory device. Pet. 3, 12–13; 615 IPR, Paper 1, 13–14.

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Patent Owner counters that, “[r]ead in context, the embodiments described with reference to Table 1 refer to transmitting a command signal to one of the multiple memory devices in the selected rank.” Prelim. Resp. 8. On this record, we disagree with Patent Owner’s interpretation of this passage. The ’912 patent states that Table 1 is a logic table “for the selection among ranks of memory devices 30 using chip-select signals.” Ex. 1001, 7:56–58. We see nothing in Table 1 that indicates a further selection of memory devices within each rank. On this record, and for purposes of institution, we agree with Petitioner that the ’912 patent’s description of sending the command signal “to only one memory device or the other memory device” by reference to logic showing the selection of one rank or another tends to show that a rank may have one memory device. *See* Pet. 12–13.

At least for this preliminary decision, we determine that “rank” refers to “one or more memory devices.” We do not construe the term further at this time. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). The parties are not precluded from arguing the proposed construction of “rank” in subsequent briefing at trial. Our final claim construction, if any, will be determined on the full record at trial.

B. Alleged Obviousness Based on Ellsberry

1. Petitioner’s Contentions

Petitioner contends that claim 16 would have been obvious based on the teachings of Ellsberry. Pet. 60–101. Petitioner represents that the Petition “is substantively identical to” the petition in the 615 IPR. Motion 1. We addressed this ground in the 615 IPR and determined that the petitioner showed “a reasonable likelihood that claim 16 of the ’912 patent is

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unpatentable as obvious over Ellsberry.” 615 IPR, Paper 20 at 50–58.

Because the Petition is identical to the petition in the 615 IPR with respect to the Ellsberry obviousness ground, we refer to the analysis in the 615 IPR Institution Decision. Below, we address the arguments that Patent Owner raises as to the Ellsberry ground in its Preliminary Response.

2. *Prior Art Status of Ellsberry*

In an *inter partes* review, a petitioner “may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications.” 35 U.S.C. § 311(b). Patent Owner argues that “documents are ‘printed publication’ prior art only as of the date they became published and available to the public.” Prelim. Resp. 44. Patent Owner argues, therefore, that Ellsberry is not a prior art printed publication under 35 U.S.C. § 311(b) because it “was not published until December 2006, after the invention date.” *Id.* at 51.

We disagree with Patent Owner’s statutory interpretation. Ellsberry is a printed publication, having been published in December 2006, as Patent Owner acknowledges. *See* Ex. 1037, code (43) (publication date of Dec. 7, 2006); *see also* Prelim. Resp. 51 (acknowledging publication date). On this record, as explained below, we are persuaded by Petitioner’s contentions that Ellsberry is prior art at least under 35 U.S.C. § 102(e)(1), having been “an application for patent, **published** under section 122(b), by another filed in the United States before the invention by the applicant for patent.” *See* Pet. 1–4 (asserting a priority date of no earlier than July 1, 2005, for claim 16 of the ’912 patent); *see also* Ex. 1037, code (22) (filing date of June 1, 2005). Thus, Petitioner asserts a permissible ground of unpatentability under 35 U.S.C. § 311(b) because it argues that claim 16 is unpatentable under 35 U.S.C.

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§ 103(a) on the basis of prior art (Ellsberry), which is a printed publication. *See Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1374 (Fed. Cir. 2022) (“[T]he ‘patents or printed publications’ that form the ‘basis’ of a ground for *inter partes* review must themselves be prior art to the challenged patent.”).⁵

The application for the ’912 patent was filed on September 27, 2007, as a continuation of U.S. Patent Application No. 11/173,175 (“’175 application”) filed on July 1, 2005, and the ’175 application is a continuation-in-part of an application filed on March 7, 2005, which issued as U.S. Patent No. 7,286,436 B2 (“the ’436 patent”). Ex. 1001, code (63). The ’912 patent also claims the benefit of the filing dates of three provisional applications filed in 2004. *Id.* at code (60), 1:6–16.

Petitioner contends that the ’912 patent cannot claim the benefit of a filing date earlier than July 1, 2005, because none of the applications filed before this date provides support for the full scope of claim 16, and Petitioner identifies various claimed features that allegedly lack support in the earlier applications. Pet. 1–4. Petitioner contends that Ellsberry, which was filed June 1, 2005, is prior art under §§ 102(a) and (e). *Id.* at 19.

⁵ *Qualcomm*, 24 F.4th at 1375 held that applicant admitted prior art (“AAPA”) cannot be the basis of a ground of *inter partes* review because it is not contained in a document that is a prior art patent or prior art printed publication. The court indicated that, in creating *inter partes* review, Congress sought to design a streamlined administrative proceeding avoiding the more challenging types of prior art identified in § 102, such as commercial sales and public uses. *Id.* at 1376. Compared to such prior art, a published patent application carries the reliability of having been published by the Office as filed, and the scope and content of what it discloses is generally well defined. As such, a published patent application that is prior art under 35 U.S.C. § 102 constitutes a document that is a prior art printed publication that may be used under 35 U.S.C. § 311(b).

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Patent Owner responds that the limitations identified by Petitioner have written description support in applications filed before July 1, 2005. Prelim. Resp. 51–65. At this stage, Patent Owner’s showing is insufficient for the reasons explained below.

Ellsberry has a filing date of June 1, 2005, which is before the September 27, 2007, filing date of the ’912 patent and also before the July 1, 2005, filing date of the ’175 application. Therefore, to antedate Ellsberry, Patent Owner must show that each application back to at least the ’436 patent, which has a filing date of March 7, 2005, provides written description support for the subject matter of claim 16. “[T]o gain the benefit of the filing date of an earlier application under 35 U.S.C. § 120, each application in the chain leading back to the earlier application must comply with the written description requirement of 35 U.S.C. § 112.” *Zenon Env’t, Inc. v. U.S. Filter Corp.*, 506 F.3d 1370, 1378 (Fed. Cir. 2007) (quoting *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1571 (Fed. Cir. 1997)); *see also In re Hogan*, 559 F.2d 595, 609 (CCPA 1977) (“[T]here has to be a continuous chain of copending applications each of which satisfies the requirements of § 112 with respect to the subject matter presently claimed.” (quoting *In re Schneider*, 481 F.2d 1350, 1356 (CCPA 1973)) (alteration in original).

Patent Owner’s arguments address only particular limitations of claim 16 and do not show that each application back to and including the application for the ’436 patent satisfies the requirements of 35 U.S.C. § 112 for all subject matter recited in claim 16. Petitioner has satisfied its initial burden to put forth a printed publication that is prior art because Ellsberry has a filing date that predates the ’912 patent’s filing date. *See Dynamic Drinkware, LLC, v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1379–80 (Fed. Cir. 2015) (“Dynamic also had the initial burden of production, and it satisfied

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that burden by arguing that Raymond anticipated the asserted claims of the '196 patent under § 102(e)(2).”). Although the burden of persuasion for proving unpatentability never shifts to Patent Owner, the burden of production shifts to Patent Owner to show that Ellsberry is not prior art, if Patent Owner chooses to argue this. *See id.*

On this record, therefore, we are persuaded that Ellsberry is prior art at least under 35 U.S.C. § 102(e)(1).

3. *Patent Owner's Arguments as to Ellsberry*

Claim 16 recites “wherein the command signal is transmitted to only one DDR memory device at a time,” which the parties identify as limitation 16.e. *See* Pet. 99; Prelim. Resp. 66.

Patent Owner argues that Ellsberry does not disclose or suggest single-device “ranks” and thus does not transmit a command signal to “only one DDR memory device.” Prelim. Resp. 66–74. Specifically, Patent Owner points to the embodiments of Figures 2, 6, and 11 of Ellsberry as having different data groups with ranks each having multiple memory devices. *Id.*, 66–70. Ellsberry teaches as follows:

FIGS. 10, 11, 12 and 13 illustrate different configurations of memory modules (e.g., DIMMs) that can be built using combinations of the control unit and bank switch according to various embodiments of the invention.

Ex. 1037 ¶ 21. Ellsberry thus refers to the embodiment of Figure 12 as a “memory module.” Ellsberry’s Figure 12 is reproduced below:

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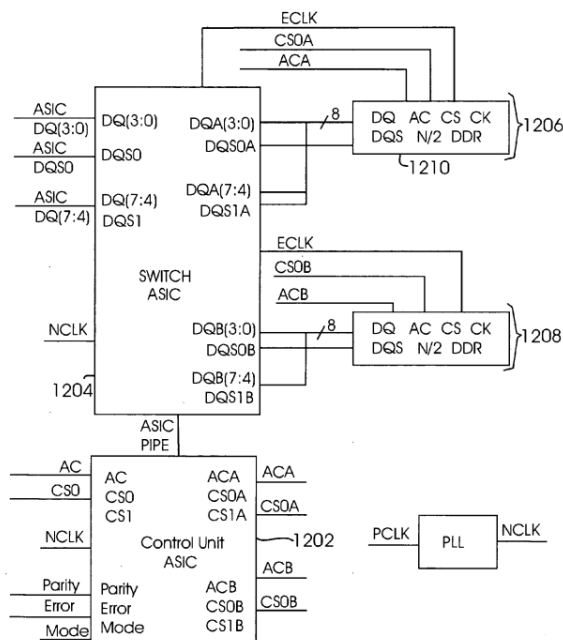


Fig. 12

Ex. 1037. Ellsberry describes Figure 12 as “a single chip-select memory configuration in which one control unit 1202 and one bank switch 1204 are used to control two memory banks 1206 & 1208, each memory bank having one memory device 1210.” *Id.* ¶ 55. Patent Owner does not explain sufficiently why “a memory bank having one memory device” is not the same thing as a single-device rank. Instead, Patent Owner focuses on JEDEC standard bit widths, Dr. Wolfe’s testimony, and the perspective of a POSITA in asserting that there were “no eight-bit-wide memory modules with the claimed DDRx devices on them as Petitioner now contends.” Prelim. Resp. 70. However, the Jacob textbook discloses 4-bit, 8-bit, and 16-bit wide data buses for SDRAMs. Ex. 1033, 370. As shown in Ellsberry’s Figure 12, either the command signal CS0A or CS0B are sent to respective memory banks 1206, 1208 each having one memory device 1210. Accordingly, in Ellsberry, “the command signal is transmitted to only one DDR memory device at a time” as recited in claim 16.

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Patent Owner further argues that a goal of Ellsberry is to reliably comply with industry standards. Prelim. Resp. 70 (citing Ex. 1037 ¶ 9). Patent Owner takes Ellsberry’s statement out of context. The full statement is that “while FET switches have a fast propagation delay, their switch time is too slow and imprecise to reliably comply with industry standards, such as the Joint Electron Device Engineering Council (JEDEC) standards, used in many memory applications.” Ex. 1037 ¶ 9. This statement, which is made in reference to the disclosure of a prior art reference, teaches to avoid FET switches if it is desired to reliably comply with JEDEC standards.

Patent Owner further argues that Ellsberry aims to “expand[] the memory capacity of a memory module” and that reducing the number of devices per rank (to one device per rank) would reduce rather than expand the capacity of the memory module. Prelim. Resp. 71 (citing Ex. 1037 ¶ 10). As shown in Ellsberry’s Figure 12, however, the bank switch enables two memory devices 1206, 1208 to be used, thereby expanding capacity without increasing load.

4. Reasonable Likelihood Determination

We have considered Petitioner’s contentions and Patent Owner’s arguments, and, for the reasons discussed above and those in the 615 IPR Institution Decision, we determine that Petitioner has established a reasonable likelihood that it will prevail in showing that claim 16 is unpatentable as obvious over Ellsberry. *See* 615 IPR, Paper 20 at 50–58.

C. Joinder

The statute governing *inter partes* review joinder states the following:

JOINDER.—If the Director institutes an *inter partes* review, the Director, in his or her discretion, may join as a party to that *inter partes* review any person who properly files a petition under section 311 that the Director, after receiving a preliminary

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response under section 313 or the expiration of the time for filing such a response, determines warrants the institution of an inter parties review under section 314.

35 U.S.C. § 315(c).

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

As discussed above, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to the Ellsberry obviousness ground. We also determine that the Petition “warrants the institution of an inter parties review under section 314,” as set forth in 35 U.S.C. § 315(c). Because Petitioner seeks to join the 615 IPR and has satisfied the requirement of 35 U.S.C. § 315(c) to file a petition that warrants institution, we do not reach Patent Owner’s remaining arguments with respect to the grounds based on Perego-422 and the Perego-422 and Amidi combination.

As discussed above, Petitioner’s Motion is unopposed by Samsung and Patent Owner. We have reviewed the Motion, and we determine that it is appropriate under these circumstances to join Petitioner as a party to the 615 IPR.

III. ORDER

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Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, an *inter partes* review is hereby instituted on the challenges raised in the Petition;

FURTHER ORDERED that Petitioner's Motion for Joinder with IPR2022-00615 is *granted*, and Petitioner is hereby joined as a petitioner in IPR2022-00615;

FURTHER ORDERED that the grounds on which trial in IPR2022-00615 were instituted are unchanged, and no other grounds are added in IPR2022-00615;

FURTHER ORDERED that Petitioner's role in IPR2022-00615 shall be limited as stated by Petitioner in the Motion for Joinder (Paper 1 at 6–9) unless and until Samsung is terminated from that proceeding;

FURTHER ORDERED that the case caption in IPR2022-00615 shall be changed to reflect joinder of Petitioner in accordance with the attached example;

FURTHER ORDERED that a copy of this Decision be entered into the record of IPR2022-00615; and

FURTHER ORDERED that all further filings shall be made in IPR2022-00615.

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SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,⁶
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⁶ Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00203 and have been joined as petitioners in this proceeding.